Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for efficiently performing parallel processing of high-speed single-bit samples comprising:

a single-bit sampler for converting an analog signal into serial single-bit samples;

a serial-to-parallel converter for converting the single-bit samples from the single-bit sampler into parallel single-bit samples; and

a digital quadrature mix for performing real-to-complex conversion, filtering, and decimation-by-two of the parallel single-bit samples from the serial-to-parallel converter and for providing parallel in-phase (I) and quadrature (Q) output values;

a filter and decimate stage to filter and decimate the parallel I and Q single-bit output values, wherein said filter and decimate stage comprises a boxcar decimation filter comprising a plurality of filter and decimate functions, wherein each of said plurality of filter and decimate functions comprise:

a NOR gate having two inputs connected to outputs of said digital quadrature mix; and

an exclusive NOR gate having two inputs connected to the two inputs of the NOR gate.

2. (Original) The apparatus for efficiently performing parallel processing of high-speed single-bit samples of claim 1 wherein said digital quadrature mix performs an Fs/4 mix wherein Fs is the sample rate.

3. (Original) The apparatus for efficiently performing parallel processing of high-speed single-bit samples of claim 2 wherein said digital quadrature mix comprises logic operations that route and invert the parallel single-bit samples resulting in the parallel I and Q single-bit output values.

4-11. (Canceled)

12. (Currently Amended) Apparatus for efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate comprising:

a serial-to-parallel converter for converting the single-bit samples into parallel single-bit samples; and

a digital quadrature mix for performing an Fs/4 frequency shift to the parallel single-bit samples and simultaneously performing real-to-complex conversion of the parallel single-bit samples from the serial-to-parallel converter to provide parallel in-phase (I) and quadrature (Q) output values at an Fs/4 intermediate frequency (IF);

a filter and decimate stage to filter and decimate the parallel I and Q single-bit output values, wherein said filter and decimate stage comprises a boxcar decimation filter comprising a plurality of filter and decimate functions, wherein each of said plurality of filter and decimate functions decimate-by-two and comprise:

a NOR gate having two inputs connected to outputs of said digital quadrature mix; and

an exclusive NOR gate having two inputs connected to the two inputs of the NOR gate.

13. (Original) The apparatus for efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate of claim 12 wherein the serial-to-parallel converter comprises shift register stages that provide a memory for use in functional realization of a boxcar filter and decimation stage in the digital quadrature mix.

14. (Original) The apparatus for efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate of claim 12 wherein said digital quadrature mix comprises logic operations that route and invert the parallel single-bit samples resulting in the parallel I and Q single-bit output values.

15-17. (Canceled)

18. (Currently Amended) The apparatus for efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate of claim 12 [[16]] wherein each of said plurality of filter and decimate functions decimate-by-four and comprise logic cells that form a two's complement three-bit output from four input bits.

19. (Currently Amended) The apparatus for efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate of claim 12 [[16]] wherein each of said plurality of filter and decimate functions decimate-by-eight and comprise two decimate-by-four functions with the outputs of said decimate-by-four functions combined in a three-in four-out adder.

20. (Canceled)